III Semester [VLSI Design & Embedded Systems]

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12EC009

M.Tech. Degree Examination, Dec. 2013 / Jan 2014.
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Draw the transfer plot of CMOS inverter. Discuss the effect of aspect ratio on the transfer curve, with suitable mathematical analysis. **(08 Marks)**

b. Derive the expression for the drain to source current in MESFET below pinch off. State the assumptions made. **(08 Marks)**

c. Bring out the differences between BiCMOS and CMOS technology. **(04 Marks)**

2 a. Explain the basic principles of modulation doping with the help of band diagrams and explain the operation of HEMT device structure formed using GaAs and AlGaAs. **(10 Marks)**

b. Derive an expression for the pinch off voltage in a MESFET. **(04 Marks)**

c. An n – channel Si JFET has Z = 24 μm, L = 4μm , a = 1.2μm and $N_a = 10^{19}cm^{-3}$, $N_d = 5 \times 10^{15}\ cm^{-3}$ and $\mu_n = 1200cm^2$ / (VS). Assume the gate voltage is -3V. Determine i) the drain current at saturation ii) the drain voltage of saturation. **(06 Marks)**

3 a. List the properties of ideal MIS system under equilibrium. **(04 Marks)**

b. Describe a typical Management Information System Structure. Also describe the energy band diagram for an ideal n – type MIS structure biases in accumulation, depletion and inversion. **(10 Marks)**

c. Describe the small signal model for a MOSFET. Also calculate the trans conductance of a MOSFET, given that L = 5μm , Z = 50μm, $V_G = 2V$, $V_{threshold} = 0.98V$, $\mu_n^1 = 500cm^2/(VS)$ $C_i = 115\ nF/cm^2$. **(06 Marks)**

4 a. A p – channel standard Si MOSFET is doped with Nd = $10^{15}\ cm^{-3}$. The MOSFET has an oxide thickness of 8nm , Z/L = 20, hole mobility = $450cm^2/(VS)$ and $Q_i = 5 \times 10^{11}q\ c/cm^2$. Given $n_i = 10^{10}cm^{-3}$, $K_i = 3.9$, $K_{si} = 11.8$ and $\phi_{ms} = -0.312$. Determine i) the threshold voltage of the device ii) the value of V_D, sat at $V_G = -2V$ iii) the value of V_D, sat at $V_G = -7V$ iv) the magnitude of the saturation current for $V_G = -1V$. **(08 Marks)**

b. Explain the sealing theory. **(06 Marks)**

c. Explain the two – dimensional potential profile for i) long channel MOSFET device and ii) short – channel MOSFET device. **(06 Marks)**

5 a. With the help of neat sketch, explain the construction and working of Carbon Nano tube FET. What are the advantages and disadvantages? **(08 Marks)**

b. Describe the defect tolerant computing. **(08 Marks)**

c. Sketch the SOI and bulk MOSFET structures and show the differences between them. **(04 Marks)**

6 a. What is the need for super buffers? Explain NMOS inverting and non – inverting super buffers with the help of i) Schematic diagrams and ii) Stick diagrams for the same. **(10 Marks)**

b. Construct 2 input NAND and NOR gates using NMOS pass transistor logic. **(04 Marks)**

c. What s a general function block? Implement 2 input EXOR gate using NMOS functional block. **(06 Marks)**

7 a. Show the implementation of the following both in circuit diagram and in stick form :
   i) NAND – NAND implementation of Y = ab + cd (only stick form)
   ii) Static CMOS AOI technology of $Y = \overline{AB+CD}$. **(04 Marks)**

b. What is tally circuit? Construct stick diagram of 3 input pass transistor tally circuit. **(06 Marks)**

c. Explain the implementation of 4 to 1 multiplexer using CMOS transmission gates. **(06 Marks)**

d. Explain global routing and local routing. **(04 Marks)**

8 a. Explain the terms hierarchy , regularity , modularity and locality as applied to integrated circuit structure design. **(10 Marks)**

b. Write explanatory note on :
   i) Programmable logic structure ii) Gate array standard cell design. **(10 Marks)**

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